Claim 6 recites a manufacturing process for a silicon epitaxial wafer. The process includes the step of forming an epitaxial layer on a silicon substrate with an interstitial oxygen concentration in a range of from 4 x $10^{17}/cm^3$ to 10 x $10^{17}/cm^3$ at a temperature of 1000° C or higher to obtain a silicon epitaxial wafer. The method also includes applying heat treatment to the silicon epitaxial wafer at a temperature in a range of from 450° C to 750° C.

In making this rejection, the Office Action took the position that the combination of Wijaranakula and Wolf discloses all of the elements of the claimed invention. However, it is respectfully submitted that the prior art fails to disclose or suggest the claimed invention, and therefore, fails to provide the advantages of the present invention. For example, the manufacturing process of the present invention is configured such that heat treatment is applied at a temperature in a range of 450°C to 750°C to an epitaxial wafer in which oxygen precipitation nuclei are reduced in an epitaxial growth step so as to form new oxygen precipitation nuclei therein.

As a result of this, oxygen precipitation proceeds in the device fabrication process subsequent to the heat treatment, especially the oxide precipitates are effectively increased, even when a wafer with a comparatively low oxygen concentration is used as a silicon substrate.

Wijaranakula discloses a semiconductor silicon wafer and a method for manufacturing a calibration wafer having a microdefect-free layer of a precisely predetermined depth. The silicon wafer is formed by depositing an epitaxial layer onto a substrate having an interstitial oxygen concentration suitable for precipitating oxide. As shown in Figures 1-3, the semiconductor silicon wafer 10 comprises a semiconductor

silicon substrate 12 that contains multiple oxide microdefects 14 and a microdefect-free layer 16 having a precise thickness 18 and extending from a front surface 20 of a semiconductor silicon wafer 10. The semiconductor silicon substrate 12 can be either intrinsic (having the conductivity of pure silicon) or extrinsic (having its conductivity changed by an added dopant such as boron, phosphorus, antimony, carbon or arsenic). The concentration of the added dopant is preferably less than 300 ppma.

Figure 4 of the reference illustrates the method of producing the wafer shown in Figures 1-3. Process step 42 indicates that an ingot of single crystal is grown. The specification states that it is grown using a Czochralski process. The growth process is such as to ensure that the resulting crystal ingot contains sufficient dissolved oxygen. The amount of dissolved oxygen is typically between 10 ppma and 50 ppma for forming microdefects 14. In process step 44, the ingot is sliced into semiconductor silicon wafers and polished. The polished wafer forms a semiconductor silicon substrate 12 ready for process step 46, which entails depositing an epitaxial layer preferably by chemical vapor deposition. The epitaxial layer contains no sites or nuclei to form oxide microdefects during subsequent annealing steps and, therefore, provides a layer free of microdefects. Process step 48 shows that the semiconductor silicon substrate 12, along with the deposited epitaxial layer, is annealed at a temperature suitable to nucleate oxide microdefects. The temperature is preferably between 600°C and 900°C. Process step 50 shows that the semiconductor silicon substrate 12, along with the deposited defect free epitaxial layer, is annealed at a temperature to grow the oxide microdefects 14 that were nucleated in step 48 in the substrate 12.

Wolf discloses specifications for silicon wafers for VLSI manufacturing.

The Office Action took the position that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wijaranakula with the teachings of Wolf because Wolf discloses temperatures of epitaxial growth, oxygen concentrations, and resistivity of boron and antimony-doped Si. The Office Action further asserted that it would have been obvious to one of ordinary skill in the art to form an Si epitaxial wafer doped with boron (or antimony or arsenic) at a temperature of 1000°C or higher on an Si substrate having an oxygen concentration of 4×10^{17} to 10×10^{17}, and then heat treating the wafer at a temperature from 450°C to 750°C, as recited in claims 6-9, because it is suggested by Wijaranakula, in light of Wolf, and "such would have been anticipated."

However, firstly, no motivation was provided as to why one having ordinary skill in the art would be compelled to modify Wijaranakula in the manner suggested. Secondly, Applicant's disclosure at page 4 specifically indicates that unless the interstitial oxygen concentration is in a range of 4×10^{17} and preferably 6×10^{17} atoms/cm^3, an oxygen concentration precipitation nucleus is hard to be formed. If the interstitial oxygen concentration exceeds 10×10^{17} atoms/cm^3, too many oxygen precipitation nuclei are formed. Therefore, Applicant's specification demonstrates that these features have a specific purpose and are not mere design choices.

Thus Wijaranakula or Wolf, either alone or in combination, fail to disclose or suggest a process for manufacturing a silicon epitaxial wafer including the steps of forming an epitaxial layer on a silicon substrate with an interstitial oxygen concentration in a range of from $4 \times 10^{17}/cm^3$ to $10 \times 10^{17}/cm^3$ at a temperature of 1000° C or higher to

obtain a silicon epitaxial wafer, and applying heat treatment to the silicon epitaxial wafer at a temperature in a range of from 450° C to 750° C, as recited in claims 6-9.

The Office Action further asserted that it would have been obvious to one of ordinary skill in the art at the time of the invention that the resistivity of such a wafer would include a range of 0.02 ohm-cm or lower because such is disclosed by Wolf on page 26, as known to be a function of doping concentration.

An object of the present invention is to provide a novel manufacturing process for an epitaxial wafer having internal gettering ability. Claims 10-13 further recite that the substrate resistivity of the epitaxial layer is 0.02 Ω-cm or lower. This substrate concentration is preferable in order to attain the desired effect of the present invention. Fig. 2 of the present invention shows the relationship between the heat treatment temperature and the bulk density after epitaxial growth. The bulk density rises depending on the temperature. As discussed in Applicant's specification the lower the resistivity, the higher the effect of the heat treatment. Fig. 2 shows that when using a P-type silicon substrate with a resistivity 0.016 Ω-cm and 0.008 Ω-cm, the bulk defect density is much higher than that with a 10 Ω-cm resistivity, after performing the heat treatment at a temperature between 450°C and 750°C. Additionally, it is known that using an N-type silicon substrate with 0.02 Ω-cm or lower, oxygen is hard to be precipitated therein. However, according to the present invention, even if using an N-type silicon substrate, the bulk defect density can be increased.

Wolf, by contrast, only teaches the range of resistivity which can be used to manufacture a mere normal silicon wafer. Wolf is silent on increasing the bulk defect

density of an epitaxial wafer or producing an epitaxial wafer having remarkable internal gettering ability, which are benefits of the claimed invention.

The epitaxial wafer of Wijaranakula is useful as a calibration wafer for measurement of thickness of a microdefect-free layer (Abstract), while an epitaxial wafer of the present invention is for a device fabrication process. As a result, the epitaxial wafer of Wijaranakula includes a bulk region having large, uniformly distributed oxide microdefects (column 3, lines 39-42). Furthermore, Wijaranakula teaches after growing an epitaxial layer, the semiconductor silicon substrate is annealed at a temperature preferably between 600°C and 900°C for longer than 24 hours, preferably between 48 and 72 hours (column 5, lines 33-38). On the other hand, since the epitaxial wafer of the present invention is for a device fabrication process, in view of productivity, the heat treatment time is within 24 hours, which is also a benefit of the claimed configuration.

Thus Wijaranakula or Wolf, either alone or in combination, fail to disclose or suggest that the substrate resistivity of the epitaxial layer is 0.02 Ω-cm or lower, as recited in claims 10-13.

Still further, because claims 7-21 are dependent on claim 6, Applicant submits that each of these claims recites subject matter that is neither disclosed nor suggested by the cited prior art, for at least the reasons set forth above with respect to claim 6.

Therefore, it is respectfully submitted that the Applicant's invention, as set forth in claims 6-21, is not obvious in view of any combination of Wijaranakula and Wolf within the meaning of 35 U.S.C. § 103.

In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claims 6-21, and the prompt issuance of a Notice of Allowability are respectfully solicited.

Should the Examiner believe anything further is desirable in order to place this application in better condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 107242-00024.**

Respectfully submitted,
ARENT FOX KINTNER PLOTKIN & KAHN PLLC

Lynne D. Anderson
Attorney for Applicant
Registration No. 46,412

27931

Enclosures: Associate Power of Attorney

1050 Connecticut Avenue, NW, Suite 400
Washington, DC 20036-5339
Telephone: (202) 857-6000

GEO:LDA/cvj